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Application Number	<del>Unknown</del> 10/796,552
Filing Date	March 8, 2004
First Named Inventor	Prasenjit Biswas
Art Unit	<del>Unknown</del> 2181
Examiner Name	<del>Unknown</del> W. TREAT
Attorney Docket Number	43496.00014

[illegible][illegible]

8/29/06

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Substitute for form 1449B/PTO		<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>		Application Number	Unknown 10/796,552
		Filing Date	March 8, 2004
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(Use as many sheets as necessary)			
Sheet	2	of	2

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
WMT		SMITH, James E. et al.; "Implementing Precise Interrupts in Pipelined Processors"; IEEE Transactions on Computers; May 1988; pages 562-573; Vol. 37, No. 5.	
		HASEGAWA, Atsushi et al.; "SH3: High Code Density, Low Power"; IEEE Micro; December 1995; pages 11-19.	
		TURLEY, Jim; "Hitachi Adds FP, DSP Units to SuperHC Chips - Two New Additions Aimed at Boosting Lead in Consumer Electronics"; Microprocessor Report; December 4, 1995; pages 10-11.	
		JOHNSON, Mike; "Superscalar Microprocessor Design"; Prentice Hall; 1991; 7 pages.	
		MARGULIS, Neal; "i860 Microprocessor Architecture"; Osborne McGraw-Hill; 1990; pages 27, 37-41, 45-53, 80-94 and 205-210.	
WMT		iAPX 86/88, 186/188 User's Manual Hardware Reference; Intel; Order No. 210912-001; 3 pages, including page 3-8 (8087 Numeric Processor Extension).	

Examiner Signature	W. TREAT	Date Considered	8/29/06
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.

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